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A process aimed at fabricating proximity x-ray lithography masks is presented. In this technique, the Ta absorber layer is deposited and patterned on the back side of the membrane and nonspin-coated electron sensitive layers were used in order to achieve high resolution patterning of this absorber. The advantages gained by this approach include a reduction of the membrane temperature during the plasma etching step of the absorber patterns without using any cooling gas. This temperature reduction results from the direct contact of the membrane with a cooling plate. This approach also allows increased protection of the absorber patterns from contamination during exposure of the mask. A third advantage is that the smooth surface of the mask exposed to the wafer in the x-ray lithography stepper may also make it possible to reduce the gap between wafer and mask, thus achieving increased resolution with the x-ray lithography process. © *2002 American Vacuum Society.* [DOI: 10.1116/1.1523399]

I. INTRODUCTION

A critical issue for increasing the resolution in proximity x-ray lithography (PXL) is keeping a minimal mask to wafer distance.[1] Recently, other researchers[2,3] have achieved 50 nm resolution with PXL by using a 10 and 15 μm gap between the mask and the wafer. Another study[4] shows that PXL can print 35 nm features using a higher energy radiation and smaller proximity gap ($\leqslant 5$ μm). Reducing the proximity gap to such a scale with standard masks however increases the risk of contact with the resist covered wafer during the positioning of the mask prior to exposure. Due to the high aspect ratio of the absorber patterns on x-ray masks, such contact can cause damage to the pattern and fractures in the membrane. Also there are risks of resist particulate contamination to the absorber patterns if contact occurs, implying the need for more frequent cleaning of the mask. However, cleaning such contaminants without any change in pattern dimension and film stress remains an unresolved issue. Alkaline solutions in the *p*H range of 10–12 are widely used to remove particles and polymer residues on W and WN*x* films in the ultralarge scale integrated manufacturing process.[5] Conventional cleaning, performed at relatively high *p*H under electrical floating condition, results in a 15 MPa stress change, and 5 nm etch depth of WN*x*.[6] Such an appreciable change in film thickness in turn gives rise to degradation of pattern accuracy of the x-ray mask.

Among the issues related to PXL mask fabrication, the membrane temperature during the plasma etch of the absorber pattern is widely regarded as one of the factors limiting the fabrication and accuracy of x-ray mask.[7] Accurate control of the membrane temperature is needed, since this parameter increases during plasma etching and uneven heat distribution across the wafer strongly affects the pattern profile and etch depth. Furthermore, uneven heat distribution can also increase the risk of membrane fracture due to mechanical stress during the etching process. An etching technique using a heat sink to control the heat distribution across the entire wafer has already been proposed by other researchers.[8] In that case, the proposed technique adds one more alignment step between the membrane area and the heat sink, and does not guarantee an equal etch rate between substrate area and the area on the membrane.

In PXL, the best resolution is obtained with the wafer as close to the mask as possible. In this geometry, the resolution R is related to the gap between the wafer and the mask g, by the relation $R=K(\lambda g)^{1/2}$, where λ is the median exposure wavelength, g the proximity gap between the mask and the wafer, and K is a constant ≈ 0.8. Any variation in the gap will cause variation in the resolution and may result in blurred images during exposure. It is clear from the previous relation that it is essential to keep the proximity gap as uniform as possible. In addition to the limitations imposed by this equation, a flow of air or helium gas between the mask and the wafer, usually used for cooling purposes during exposure, can cause turbulence in the gas flow and such turbulence can cause pressure fluctuations against the membrane.[9–11] Turbulence caused by the absorber patterns on the membrane may be eliminated by patterning on the back of the membranes. The masks fabricated using this fabrication method have a completely smooth surface on the side of the gap between the mask and the exposed wafer. Furthermore, irregularities of the gap can cause up to 20% disturbance and fluctuation in the relaxation time of a Si_3N_4 membrane since the relaxation time is inversely proportional to the third power of the mask/wafer gap value.[9] Sudden gap reduction can trap gas under the membrane, and actually delay the attainment of the equilibrium. A gap increase which is too rapid could possibly result in collision between the mask and the wafer.

To overcome these drawbacks, this article presents a process related to a recently developed approach for obtaining a

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uniform heat distribution across the entire mask during deposition and etching of the absorber. This technique also significantly reduces the need for cleaning the patterned area of the mask between exposures, and reduces the irregularities inside the wafer/mask gap in a PXL stepper during exposure by having the mask present a smooth surface toward the wafer. In using this technique, the patterning of the absorber layer is done on the back side of the membrane. This is not possible using conventional electron sensitive resists since spin coating does not produce a uniform thickness layer on very high relief structures such as the back of a PXL mask, which in essence is a deep well in the silicon wafer with the membrane located at the bottom. However, the silicide direct-write electron beam lithography (SiDWEL) process[12] and electron beam resists that are not spin coated make such a fabrication scheme possible to achieve.

II. EXPERIMENT

Absorber structures were patterned on two types of samples: on silicon nitride membranes and on silicon nitride thin films deposited on small pieces of silicon ($\sim$1 cm^2). These latter samples were required in order to perform grazing angle observations of the absorber profiles with a scanning electron microscope. Both types of samples were prepared using the same processes so that aside from the back etching of the silicon to form silicon nitride membranes, both types of samples have identical film thickness, and the same thickness of silicone nitride. Furthermore, the processing of the two types of samples is also essentially identical due to the use of a low energy electron beam for pattern writing and effective mask cooling during the absorber etch, as will be described in the following section. Note that while Si_3N_4 is used in this study the method is applicable without any modification in the case of other types of membrane materials. Figure 1 shows the x-ray mask fabrication process flow used in this work. First, a Si_3N_4 film is deposited by low-pressure chemical vapor deposition on a Si wafer of 7.5 cm diameter, and the silicon wafer is back etched using a KOH solution, thus forming a membrane. A chromium etch stop layer (50 nm) and a β-tantalum absorber (350 nm) are deposited by rf sputtering on the back of the membrane. Tantalum was chosen as the absorber for its chemical stability, making it possible to perform repeated cleaning of the mask in an industrial environment.[13] Also, it has been demonstrated by other researchers[7] that Ta has excellent mechanical properties, allowing adequate image placement for the 70 nm fabrication node of the International Technology Roadmap for Semiconductors.[14] As mentioned earlier, in order to adequately pattern the absorber regions on the back of the membrane, it is required to use a nonspin coated resist. It is essential to evaporate electron-sensitive layer(s) in such a high relief structure to achieve sufficient uniformity for sub-100 nm patterning. For SiDWEL, 15 nm layers of silicon and nickel are then evaporated on top of the Ta layer. Electron beam lithography is used to form high resolution silicide structures out of the Ni and Si layers. Due to the resistance of these silicide structures to the tantalum-etching chemistry, no intermediary hard mask is needed between the electron sensitive layers and the absorber. Electron beam lithography was performed using a LEO 1530 field emission gun scanning electron microscope (FEG-SEM) externally controlled by the Nabity Pattern Generation System. A four element deformation matrix is calculated to allow stitching of 200 μm square fields with an overall accuracy of $\sim$100 nm. Both of the lithography processes described here are optimized for low electron beam energies ($<$5 keV), which avoids causing proximity effects in the patterning. At a typical energy of 3 keV, Monte Carlo simulations demonstrate that the range of the backscattered electrons is less than 20 nm.[15] The backscattered electron range is therefore less than half of the minimal distance between lines even for 70 nm 1:1 line gratings. Since most proximity effects can be attributed to back-

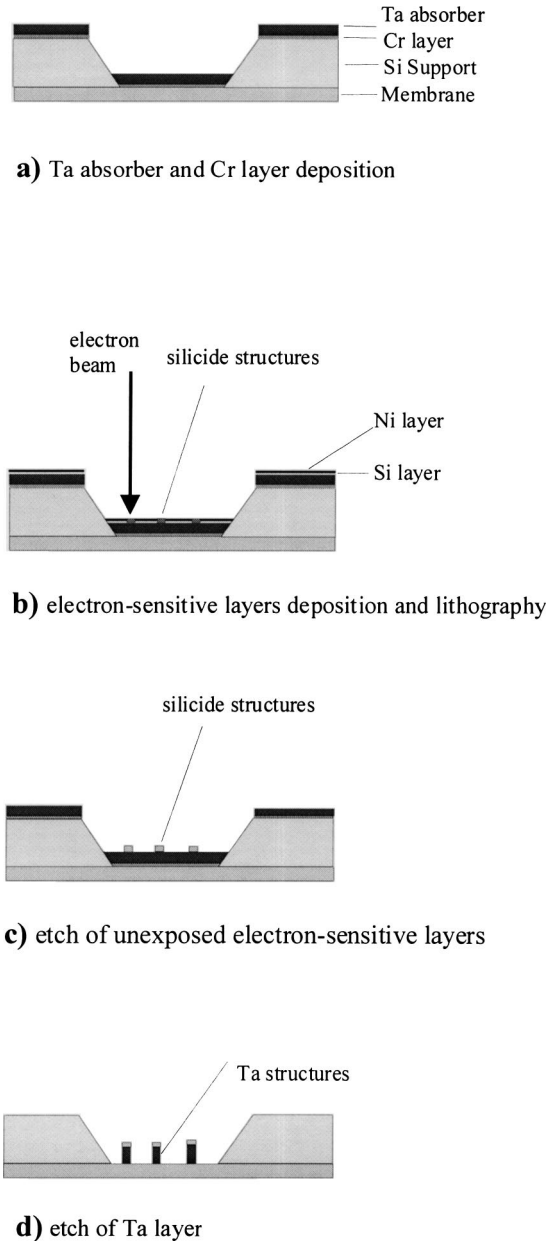

FIG. 1. X-ray mask fabrication process.

scattered electrons, this is sufficient to avoid any proximity effects due to lithography even for the most strict 70 nm design rules. Moreover, the electron source being used is a FEG which makes it possible to maintain a beam diameter better than 5 nm even at such low energy and at a beam current of 900 pA. The exposure dose depends on the materials that are used to form a silicide structure and on the beam energy as a function of the thickness of the metal and silicon layers. In the specific case of the samples prepared for this experiment where the nickel is used to form the silicide, the exposure dose is 12.8 mC/cm^2.

Development is then performed using wet acid solutions to remove the unexposed regions of Ni and Si. Line edge roughness of $3\sigma \approx 20$ nm has been achieved with resolutions of 100 nm. It has been demonstrated that the SiDWEL process itself allows the fabrication of lines as small as 30 nm. The silicide pattern is transferred to the Ta absorber using a SF_6:CH_4 mixture in a March 1701 reactive ion etching (RIE) system at a power of 80 W.

In the conventional method for the fabrication of PXL masks heating of the membrane occurs during plasma etching of the absorber layer, mainly due to the fact that the heat capacity of the membrane is very small. In order to avoid damage caused by this heating, researchers have used two level plasma chambers, providing cooling of the membrane from the back side using a helium gas flow.[16,17] Other researchers have attached heat sinks to the back side of the membrane to control the temperature of the membrane as well as the substrate during processing so that the absorber film can be etched uniformly.[8] In the approach described here, uniform heat distribution across the entire wafer is achieved without using cooling gas or heat sink. By using the proposed patterning on the back side of the membrane, we have placed the membrane itself directly on top of a water cooled metal electrode (RIE bottom electrode) during the etching process, eliminating the need for a two level chamber or cooling gas. This process can be expected to maintain a low membrane temperature and makes the control of temperature uniformity across the whole wafer a much simpler task to achieve, thereby significantly improving control over the uniformity of the absorber etch rate.

III. RESULTS AND DISCUSSION

Figure 2 shows 30 nm linewidth patterns fabricated using the SiDWEL process. Such test patterns were used to measure the resolution limits of the lithography process and the line edge roughness prior to Ta etching. Figures 3 and 4 show results of tantalum test patterns fabricated using this process on test samples. The test pattern features linewidths ranging from 250 to 117 nm after etching of the absorber. The line edge roughness on the lines is on the order of $3\sigma \sim 30$ nm. Since the SiDWEL lithography itself under the conditions used here has a line edge roughness of $3\sigma \sim 20$ nm, most of the roughness of the Ta lines can be attributed to the grain size of the Ta layer. Such roughness on β-Ta is in agreement with results from other research groups using pure Ta absorber layers.[18]

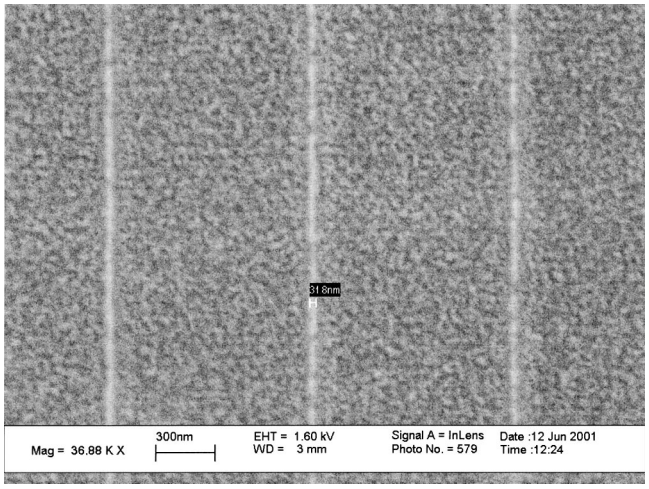

FIG. 2. SEM image of 30 nm lines achieved by the SiDWEL process.

Figure 5 shows more specifically 130 nm linewidth patterns fabricated using the SiDWEL process on the back side of the membrane, where the roughness of the surface under the absorber is due to the chromium etch stop layer. It is important to note that no dose correction or proximity pattern correction was used during exposure by the electron beam lithography and that a uniform dose was used for all the lines. The intersection of the lines demonstrates that for such resolutions, no proximity effects can be observed. Similar results have been obtained using the in-house negative resist QSR-5.

In the proposed technique, where the patterning is done on the back side of the wafer, the gap between the wafer and the mask is more uniform, and the chance of contamination of the patterned side during exposure is less than the conventional fabricated mask where the pattern is facing the wafer. Another advantage of using evaporated electron beam layers instead of conventional resists is that it is possible to deposit such resists directly on the membrane, after back etching of

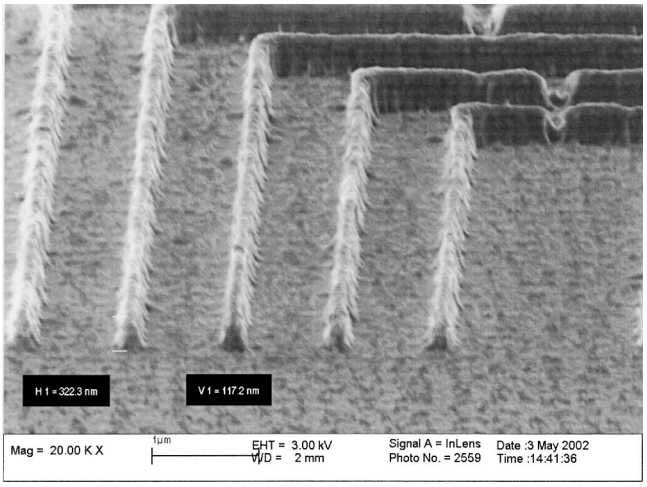

FIG. 3. SEM image of Ta absorber lines 117 nm linewidth (V1), and 322 nm height (H1) on test sample.

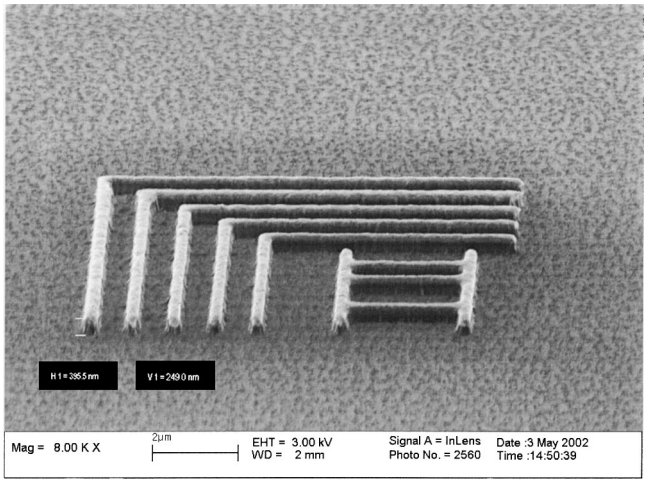

FIG. 4. SEM image of Ta absorber lines with 249 nm linewidth (V1) and 325 nm height (H1) on test sample.

the Si support wafer. No fracture of the membranes was observed after the deposition of the resist, and after completing the fabrication process.[19,20]

IV. CONCLUSION

A fabrication process, which makes it possible to pattern the x-ray absorber on the back side of the PXL mask membrane, was demonstrated. More specifically, 130 nm wide lines etched in β-Ta were fabricated with 70° sidewalls on the back of a silicon nitride membrane. The verticality of the sidewalls however is only limited by the RIE etching process, and not by the lithography process. It was also determined that the roughness of the lines was not related to the fabrication flow or to the resist patterning, but only to the absorber grain size. Thus we conclude that this back patterning of the membrane technique is a practical solution for uniform heat distribution during absorber etching. It is important to note that this fabrication flow could also be applied to x-ray masks using other absorbers such as W, TaB, or TaGe and other membrane materials such as diamond or SiC with the same benefits in term of heat distribution. Moreover, this technique reduces the need for cleaning the mask, and if cleaning is needed then it will be applied to the unpatterned side of the mask, which is much easier to apply. Further investigations are required for better understanding of relaxation time of the membrane, the deflection of x-ray mask membrane in stepper motion, and the effect of gas flow in the proximity gap between the mask and the exposed wafer in a stepper environment.

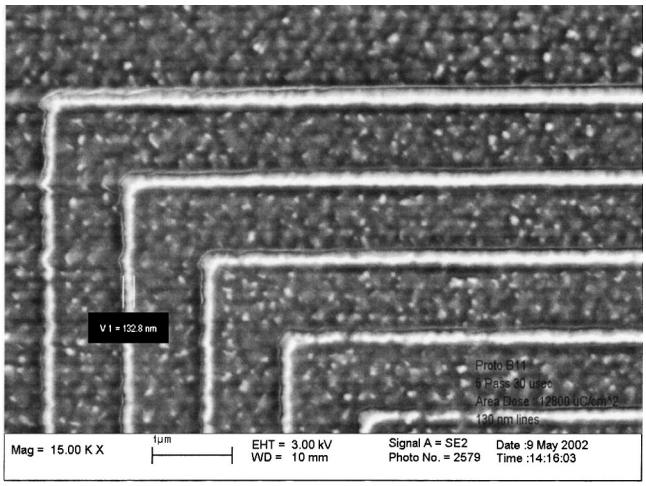

FIG. 5. SEM image of x-ray mask patterns of 130 nm linewidth Ta absorber lines fabricated on back side of membrane.

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